Conventional Art Figure 1 illustrates a typical configuration of a plan view of a section of a memory array, 100, in a common configuration for a memory device. Conventional Art Figure 1 is not drawn to scale. As shown in Conventional Art Figure 1, array 100 comprises rows 110 and columns 120 of memory cells. Each of the memory cells are isolated from other memory cells by insulating layers (e.g., a plurality of shallow trench isolation regions (STI) 112. The control gates of each of the memory cells are coupled together in each of the plurality of rows 110 of memory cells, and form a plurality of word lines 101 that extend along the row direction. Bit lines extend in the column direction and are coupled to drain regions via drain contacts 108, which are typically "vias" in an associated column of memory cells 120.

A plurality of source lines (Vss) 102 extend in the row direction and are coupled to, and comprise, the source regions of each of the memory cells in the array of memory cells 100. One source line provides the source regions in adjoining rows of memory cells, and as a result, one source region is shared between two memory cells. Similarly, drain regions are shared amongst adjoining rows of memory cells, and as a result, one drain region is shared between two memory cells.

Conventional art Figure 1B, (Section A-A) illustrates the depth relationship between STI 112, source/Vss lines 102 and drains 118. As is illustrated in Conventional Art Figure 1C, the source/Vss lines 102 are typically formed by ion implantation 150 in the silicon substrate of the memory device. The drain regions are also formed by ion implantation, 151. Because the source implantation must be formed in the substrate under the existing STI trench and between existing cells, the ion energies required are very large, on the order of $2e^{15}$ eV. In order to provide a continuous source line, the implantation beam must be angled to provide implantation in the STI trench walls. The angles are on the order of twenty degrees from vertical. The large implantation energies also form the conductive extension of the source regions under the memory cells. As cell sizes shrink, the insulative region between source and drain, 161, can narrow to the point of shorting the memory cell.

What is needed, then, is a method for forming a Vss connection that provides the requisite continuity between source regions without shrinking the isolation between source and drain. Furthermore, the method must be achievable using existing manufacturing methods.

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